containing higher level code that may be executed by the computer using an interpreter. The above-described devices may be configured to act as one or more software modules in order to perform the operations of the above-described example embodiments, or vice versa.

[0190] It should be understood that example embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each device or method according to example embodiments should typically be considered as available for other similar features or aspects in other devices or methods according to example embodiments. While some example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims.

What is claimed is:

1. A clean data strobe signal generating circuit, comprising:

a first receiver configured to receive a differential data strobe signal comprising at least a first input data strobe signal and a second input data strobe signal, and output a first single ended data strobe signal;

a second receiver configured to receive the second input data strobe signal and a reference voltage signal, and based on the received second input data strobe signal and the reference voltage signal, output a second single ended data strobe signal;

a gate signal generator configured to generate a data strobe gate signal synchronized with the first single ended data strobe signal based on the first and second single ended data strobe signals and a memory gate signal, the memory gate signal including a pulse width that varies in accordance with a burst length after termination of a read latency; and

at least one logic gate configured to receive the first single ended data strobe signal and the data strobe gate signal to generate a clean data strobe signal for receiving read data.

2. The clean data strobe signal generating circuit of claim **1**, wherein the differential data strobe signal is transmitted from a semiconductor memory device.

3. The clean data strobe signal generating circuit of claim **1**, wherein the phase of the second single ended data strobe signal is opposite to the phase of the first single ended data strobe signal except in an unknown section of the first single ended data strobe signal.

4. The clean data strobe signal generating circuit of claim **1**, wherein

the data strobe gate signal transitions to a first level in response to a signal synchronized with the second single ended data strobe signal;

the number of toggles of the first single ended data strobe signal is counted in response to a count start signal synchronized with a first falling edge of the first single ended data strobe signal; and

the data strobe gate signal transitions to a second level in response to a reset signal generated after the counting of the number of toggles.

5. The clean data strobe signal generating circuit of claim **1**, wherein when the first single ended data strobe signal is inverted by an inverter, the at least one logic gate is a NOR gate that is configured to generate a NOR response.

6. The clean data strobe signal generating circuit of claim **1**, wherein when the phase of the first single ended data strobe signal is opposite to the phase of the first input data strobe signal, the at least one logic gate is an AND gate that is configured to generate an AND response.

7. The clean data strobe signal generating circuit of claim **1**, wherein the differential data strobe signal is applied from a Low Power Double Data Rate 4 (LPDDR4) Dynamic Random Access Memory (DRAM) device configured to perform a ground voltage termination type of on-die termination operation.

8. The clean data strobe signal generating circuit of claim **1**, wherein the clean data strobe signal is provided as a data clock signal of a First-In First-Out (FIFO) memory configured to receive the read data.

9. The clean data strobe signal generating circuit of claim **1**, wherein the pulse width of the memory gate signal is half of a width of the burst length.

10. The clean data strobe signal generating circuit of claim **1**, wherein a pulse window of the data strobe gate signal when extra toggling exists in the first single ended data strobe signal becomes narrower.

11. A clean data strobe signal generating circuit, comprising:

a first receiver configured to receive a differential data strobe signal comprising first and second input data strobe signals, and output a first single ended data strobe signal;

a second receiver configured to receive the second input data strobe signal and a reference signal, and based on the received second input data strobe signal and the reference signal, output a second single ended data strobe signal;

a memory gate signal generator configured to generate a memory gate signal having a pulse width to which a burst length is applied after termination of a read latency;

a gate signal generator configured to receive the first and second single ended data strobe signals and the memory gate signal, and generate a data strobe gate signal by counting a number of toggles of the first single ended data strobe signal based on the memory gate signal; and

at least one logic gate configured to receive the first single ended data strobe signal and the data strobe gate signal, and generate a clean data strobe signal for receiving read data, as a gating response.

12. The clean data strobe signal generating circuit of claim **11**, wherein the differential data strobe signal is transmitted from a Dynamic Random Access Memory (DRAM).

13. The clean data strobe signal generating circuit of claim **12**, wherein the DRAM is a Registered Dual In-line Memory Module (RDIMM) or a Load-Reduced Dual In-line Memory Module (LRDIMM).

14. The clean data strobe signal generating circuit of claim **11**, wherein the counting of the number of toggles of the first single ended data strobe signal is performed by a counter or a shift register.

15. The clean data strobe signal generating circuit of claim **11**, wherein a pulse window of the data strobe gate signal becomes wider when extra toggling does not exist in the second single ended data strobe signal.